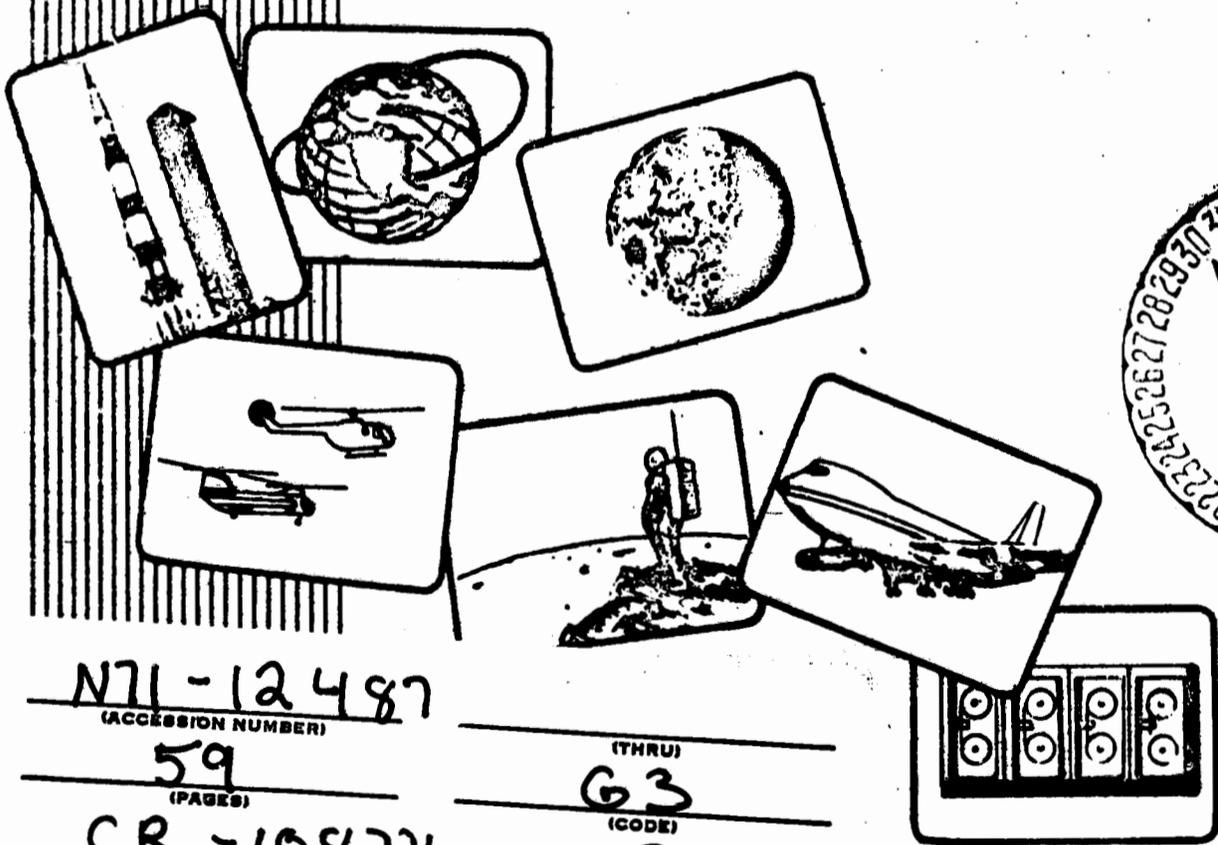


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SNEAK CIRCUIT ANALYSIS HANDBOOK



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ABSTRACT

The concepts of formal engineering analysis to detect, and thus prevent, sneak circuits are presented. Sneak circuits are commonly known as system "glitches" or electrical anomalies which are not contingent on component failures. It has been found that such sneak circuits have distinct, classifiable characteristics which make engineering analysis feasible. These characteristics and methods for their recognition are disclosed herein.

KEY WORDS...

Sneak Circuits
Pathfinding
Circuit Topology
Electrical/Electronic Analysis
Computerized Electrical System Analysis
Apollo Spacecraft Analysis
Topological Analysis
Network Trees
Node Topographs

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14. D2-118222-1A, "Regeneration-1/Automated Sneak Program (ASP)" - The Boeing Company.
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1.0 INTRODUCTION

This handbook describes a sneak circuit analysis method and its application to electrical or electronic systems. It is intended for use in initiating a sneak circuit analysis task. If the analysis is to be aided by automated circuit path tracing, then the handbook should be used in conjunction with the referenced computer program documents.

The handbook is divided into three sections. The introductory section gives some of the history of Apollo sneak circuit analysis and scopes the types of circuits to which the analysis has been applied. In the next section, Theory, a sneak circuit definition and ensuing discussion lead directly to some examples of known sneak circuits. Also described is a method of reducing system complexity to achieve selective loss of detail for analytical purposes. A new technique, topological recognition, and its use as an analytical tool is discussed, and the section is concluded with recognition clues to assist the analyst in searching for sneak circuits.

The section entitled "Application" relates the details of sneak circuit analysis based on Apollo experience but is intended for general application to any electrical or electronic system. Schematic data systems and tracking of changes to assure current configurations are discussed. Data reduction to produce network trees and, subsequently, node topographs is illustrated. Analysis of system operating modes and application of sneak circuit clues is described. The section is ended with a description of a new automated method of tracing through schematic information to find circuit paths--perhaps the most significant advance in computer application to electrical/electronic schematic information processing.

1.1 Background

During the Apollo Lunar Landing Program, officials of the National Aeronautics and Space Administration at the Manned Spacecraft Center in Houston, Texas, recognized sneak circuits as a latent type of electrical hardware deficiency which could destroy critical equipment and endanger the astronaut

crew. Accordingly, a sneak circuit analysis task was implemented on Apollo in early 1968. A team of electrical and electronic analysts and data processing specialists was assigned the task of identifying sneak circuits in the Apollo spacecraft. An additional goal established at the outset was to automate as much of the analysis as possible to remove human error and expedite results.

To date, the analysis has uncovered over 60 sneak circuits, most of which could be prevented by crew procedural changes. In addition, an operational computer program was developed to automatically search out circuit paths, thus eliminating the burdensome and costly task of tracing from one schematic page to the other in order to complete a circuit. As a by-product, many schematic errors have been found through the use of this program.

The material contained herein is based wholly on the experience gained during the first two years of performing the Apollo sneak circuit analysis task.

1.2 Purpose

This handbook has been prepared for the sole purpose of making available to all agencies the experience and techniques gained from analysis and development of sneak circuit technology on Apollo. It is primarily intended for the sneak circuit task manager and provides an overall, yet detailed, description of the sneak circuit analysis method and its application to electrical or electronic systems. Further, it gives a baseline description of the Automated Sneak Program (a computerized circuit path finder) which, in conjunction with the referenced computer documents, may be used to initiate a computer-assisted analysis. The handbook may also be used by the analyst to get a clear understanding of what a sneak circuit is and how to find it.

1.3 Scope

The scope of the handbook includes a detailed description of the theory, data, and methods required to perform a sneak circuit analysis. It emphasizes sneak circuit identification through the application of topological clues. A general description of the Automated Sneak Program is given.

The original sneak circuit analysis plan (Reference 1) identified two types of sneak circuits; current sneaks and signal sneaks. This handbook deals predominately with current sneaks in power and control circuitry. Application of the methods to digital logic circuits of computers is not the subject treated herein even though in some cases logic gates and other logic elements are included as circuit components initiating or inhibiting control functions.

2.0 THEORY OF ANALYSIS

This section treats the theoretical aspects that evolved during the course of analysis for sneak circuits on Apollo. At the outset of the analysis, not even an accurate definition of a sneak circuit existed. Later, a generally acceptable definition and some clues for finding sneak circuits were established. The clues were found empirically. For example, it was noted that latent circuit paths resulting from unusual switch configurations which connected two or more power busses or power sources together, often led to sneak circuits. In addition, switching modes that allowed current reversal through one branch of a circuit often caused a sneak circuit. These clues and others noted below were analyzed in and of themselves. The result led directly to the following analytical theory: Electrical and electronic circuits, no matter how interconnected and interrelated, can be topologically simplified using selective loss of detail, until certain sneak clue patterns can be easily recognized. Analysis of circuit operating characteristics in the pattern is used to determine sneak circuit probability.

As detailed later in this section, some latent anomalous circuit conditions do not result from sneak current paths but rather from incorrect circuit timing, false labels on controls, and ambiguous or false indications of status on meters and other readout devices. Experience has shown that these latent conditions are also more easily uncovered using topological simplification.

2.1 Sneak Circuit Definition

A sneak circuit is defined as a path that has a latent anomalous electrical condition resulting from an unapparent stimulus-response relationship which causes an unwanted function or inhibits a wanted function. It should be noted that the electrical condition includes not only electrical and electronic elements but also involves associated operator observations and resultant actions.

2.2 Sneak Circuit Example

The original example provided by NASA to illustrate a sneak circuit shows how an apparently innocent-looking circuit

can lead to a significant failure. The circuit as illustrated in Figure 2-1 shows engine ON and OFF commands to a typical missile or launch vehicle.

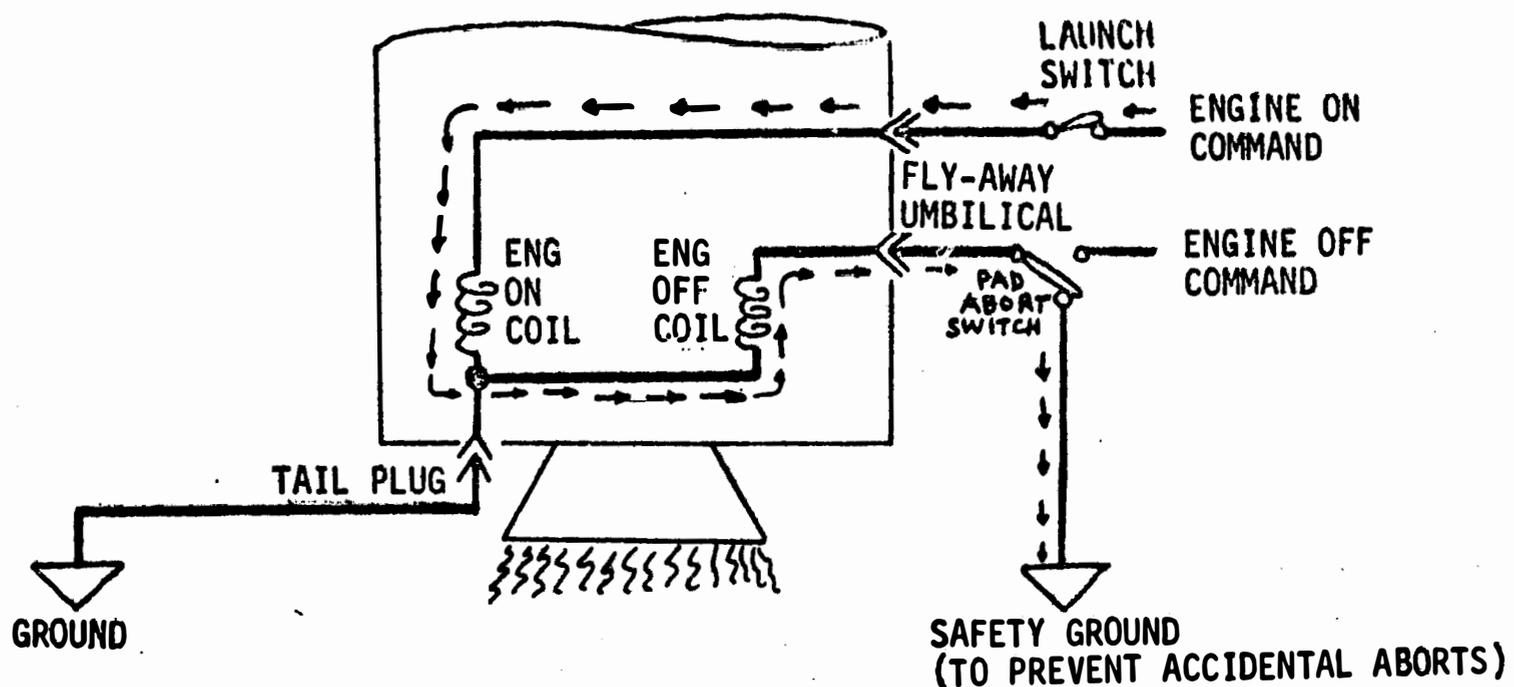


FIGURE 2-1. Original Sneak Circuit Example

The sneak path, as indicated by the arrows, occurs when the umbilical tail plug pulls out before the fly-away umbilical pulls away. This allows electrical current to flow in a reverse direction through the engine OFF coil causing engine cutoff to occur just after the vehicle has lifted off the launch pad.

2.3 Classification of Sneak Circuits

A sneak circuit can be broken down into its constituent parts in order to better understand the various possible means by which it will occur. Every sneak circuit involves a stimulus, a path, and a response, and each of these component parts may

be the initiator of an unintended action or function. The stimuli can be manual or automatic and include such actions as switch operations, relay transfers, logic enables, etc. Paths always include electrical-electronic elements permitting electrical energy flow but may also require associated non-electrical energy forms for completion. Responses include indications as well as subsequent functions which in turn may act as stimuli. Thus, a sneak circuit driving an indicator, say an abort light, can cause an unnecessary subsequent action which may have far-reaching consequences.

Sneak circuits may be classified into four categories as an aid to analysis. The four categories are based on different sneak conditions which may exist as follows:

1. Sneak Path - A sneak path may cause current or energy to flow along an unexpected route.
2. Sneak Timing - Sneak timing may cause current or energy to flow or inhibit a function at an unexpected time.
3. Sneak Indication - A sneak indication may cause an ambiguous or false display of system operating conditions.
4. Sneak Label - A sneak label may cause incorrect stimuli to be initiated.

2.4 Analytical Technique

The basis of the sneak circuit analytical technique is topological simplification of circuitry to facilitate clue pattern recognition. Thus, the first step requires that the system and detail electrical schematics be simplified to basic circuit continuities showing power sources, nodes, switches, diodes, loads, and grounds. The circuit elements and interconnections are drawn in the form of a network tree using selective loss of detail to show only the important elements. The resultant sketch is not place-oriented as are most schematics. All extraneous information is omitted including wiring data, component nomenclature,

and plug-jack identification. However, switch and circuit breaker labels are included and all plug-jack pairs that are interrupted (separated) as part of the normal mode of operation are shown as switches. Most importantly, all circuit connections must be shown to enable analysis of the complete circuit and its interactions. Functional relationships between circuit components, such as relay coils in one network tree and their contacts in another tree, are noted for composite analysis. This technique reduces a circuit found on many pages of drawings to a representation on one small sheet of paper, thus providing the system overview required for effective analysis.

Initially, all switches are shown closed in each position, and the network tree thus includes all possible current flow paths. Later in the analysis, these switches will be selectively "opened" to separate real circuits from those created by impossible switch configurations.

The type of network tree used for the analysis is illustrated below in Figure 2-2.

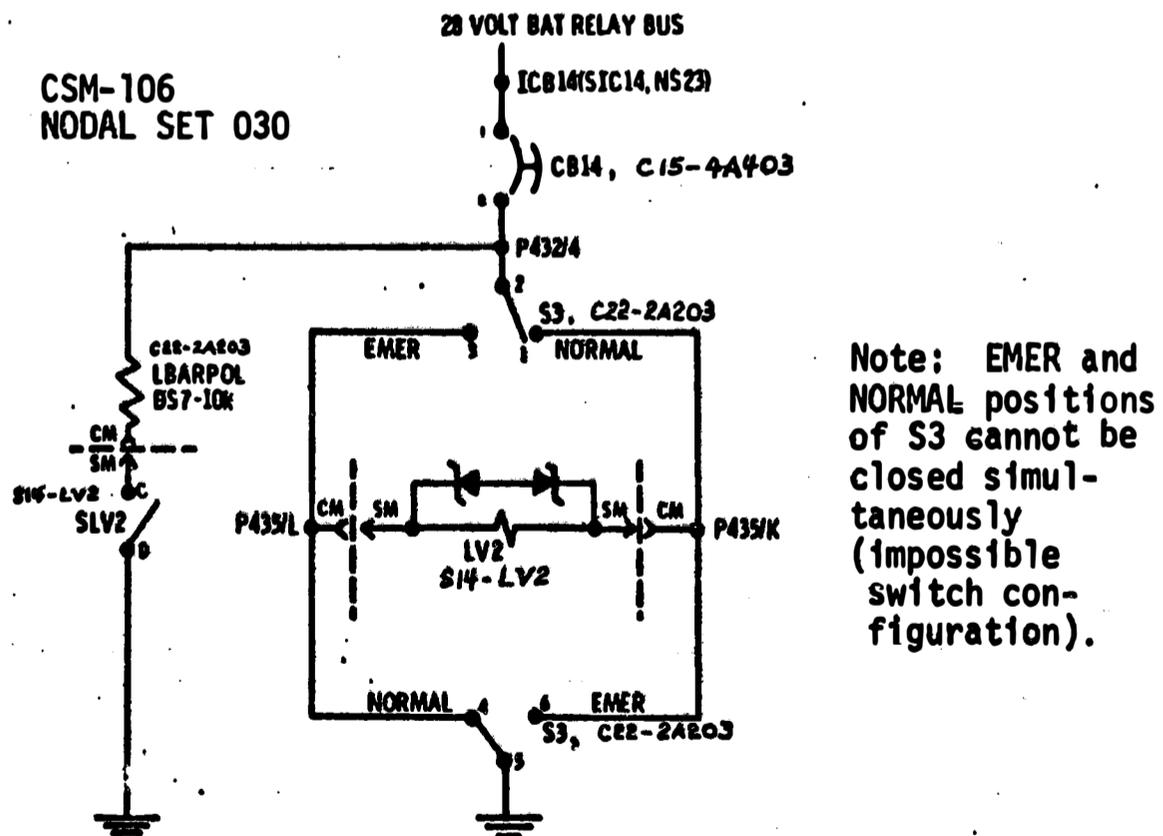


FIGURE 2-2. Example of Network Tree

2.5 Node Topographs

Each network tree is analyzed in detail for current flows by visualizing or drawing a "topograph" for each node. The topograph shows the branches attached to the node and oriented toward power or ground. The elementary node topographs are:



FIGURE 2-3. Elementary Node Topographs

In the topographs, the power source is assumed to be above the nodes, and ground is taken to be below the nodes. Each branch may have impedance, and switches are indicated by small slash marks across the branches. In the above cases, each branch is always oriented either toward power or ground with respect to the node, regardless of switching. However, in some cases a branch can change modes with respect to a node. That is, it can be oriented toward power for some switch conditions and toward ground under other conditions of switching. These cases require a special, compound node topograph:

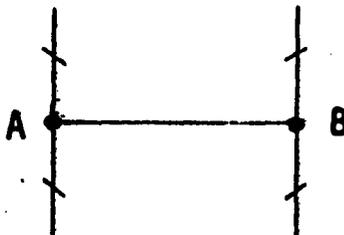


FIGURE 2-4. "H" Topograph/Reverse-Current Dome

The "H" topograph actually is the combination of a ground dome and a power dome. However, it is more descriptive as a unit because it plainly shows that branch A-B can change modes (between power and ground) with respect to nodes A and B. The most peculiar aspect of this topograph is that current can actually reverse directions through the A-B branch as different combinations of the switches are opened or closed.

The elemental topographs presented above are quite simple, perhaps deceptively so. The technique of breaking up a tree into its component node topographs is a powerful tool for analysis of even the largest of network trees. It provides an orderly method of accounting for all current flows without getting lost in complexity. Each node topograph is therefore an analysis key for application of sneak circuit clues against the network tree. Multiple branches comprising each part of a node topograph must be applied individually and in combination in the patterns. The sneak circuit clues discussed in the following section are centered around recognition of the topology presented above.

2.6 Sneak Circuit Clues

The clues given in this section are to be applied against the network trees by using the node topographs and system operation knowledge. Generally, each node topograph is to be located in the tree and used as the baseline from which to check for any possible problems. The problems will fall into one or more of the sneak circuit categories: sneak path, sneak timing, sneak indication, or sneak label.

2.6.1 Power-to-Power Path

Different voltage sources/levels may be switched into parallel through the tree (unintentional path).

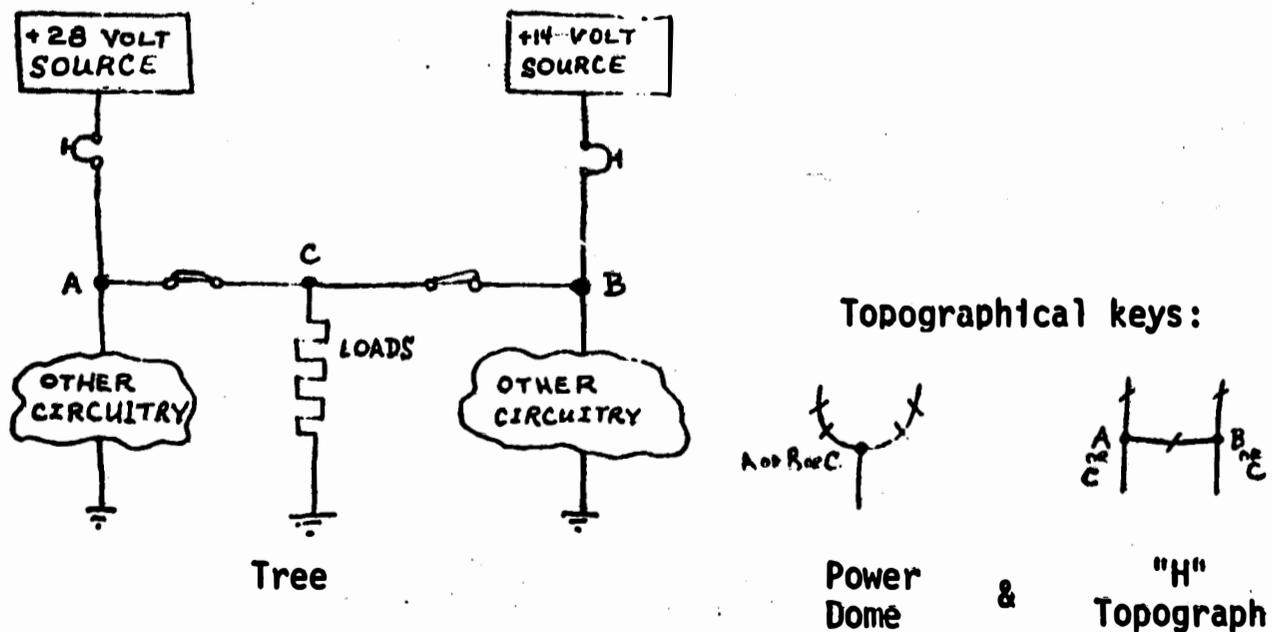


FIGURE 2-5. Power-to-Power Sneak

The power dome provides a low impedance path to the 14 volt-differential between batteries for some switch conditions in the above example.

2.6.2 Ground-to-Ground Path

The ground points of the tree may be at different absolute potentials. For example, even a ground bus may "float" off vehicle ground due to distributed impedances, thus changing the effective load voltages.

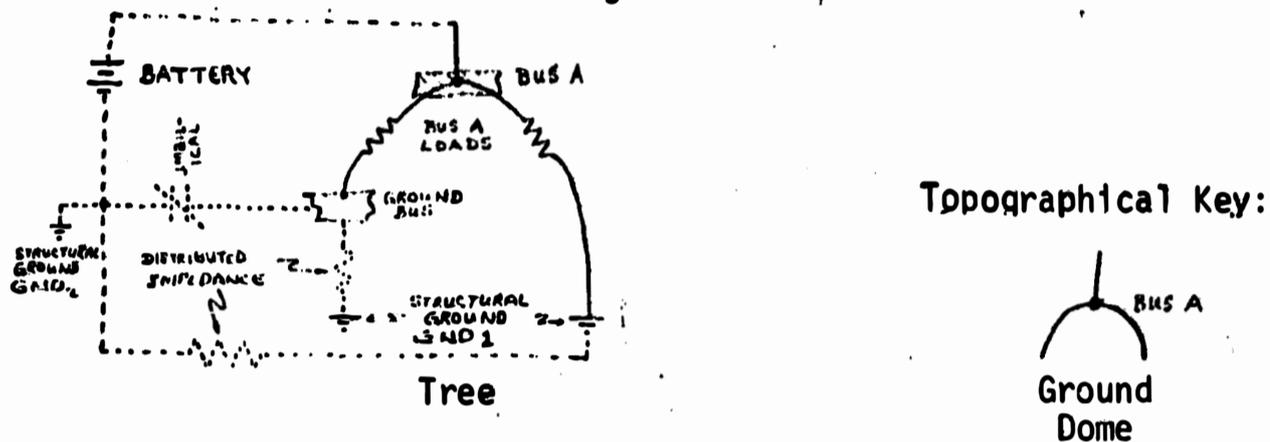


FIGURE 2-6. Ground-to-Ground Sneak

In the normal treatment of Bus A in the tree above, both the ground bus and the right-hand structure ground point are considered ground in the tree. However, the distributed impedance through structural connections can cause GND₁ to lift off zero volts, whereupon the Bus A loads do not get full voltage. This results from an unintentional path (through impedance) in the ground return circuitry.

2.6.3 Reverse Current Flow

Switching modes may allow current reversal through the cross branch of the H. The reverse current aspect of a tree is generally the most "sneaky" of all. It results from an unintentional path and/or bad timing. It can encompass misleading labels and/or ambiguous indicators.

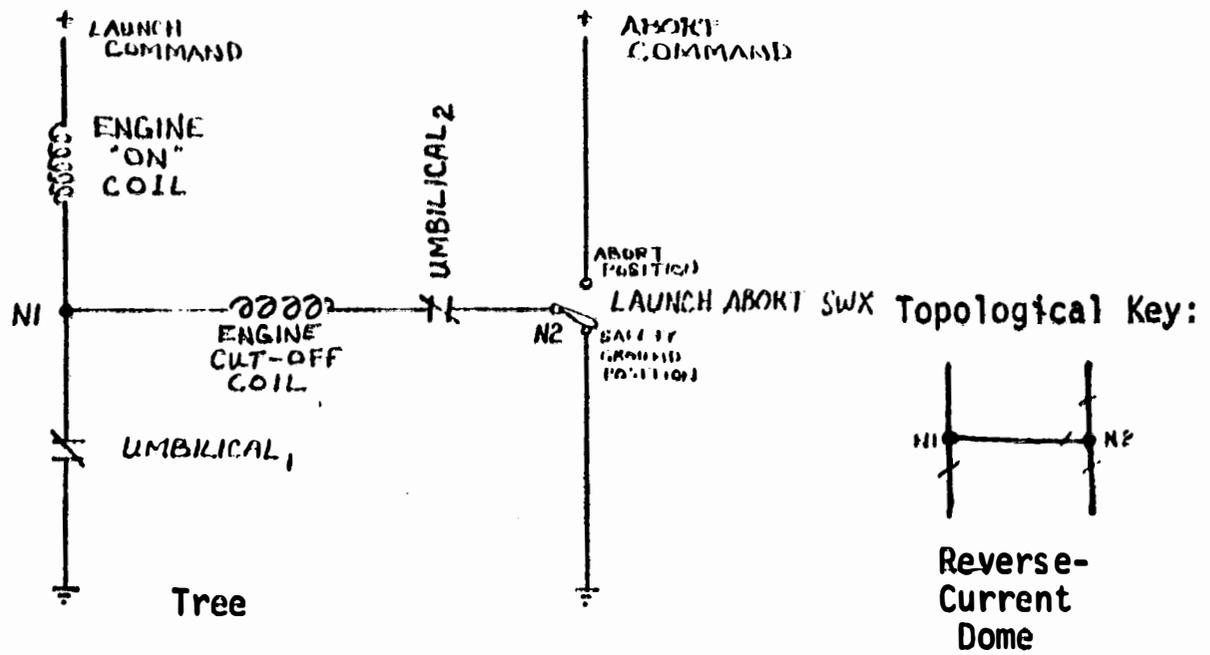


FIGURE 2-7. Reverse Current Sneak

The tree above represents the original sneak circuit example given in Figure 2-1. The "engine on" coil and the "engine cut-off" coil share a ground node at N1 through Umbilical₁. The design intent is for current to flow from N2 to N1 through the engine cut-off coil when the launch abort switch is in the ABORT mode. A safety ground is provided through the switch to prevent accidental aborts from stray line voltages. However, if Umbilical₁ opens before Umbilical₂, and if the launch abort switch is in the safety ground position, then current will reverse through the "H", going from N1 to N2 to ground. This may pick the engine cut-off coil and abort the launch unintentionally. Such a sneak circuit is a result of both an unintentional path and bad timing of the umbilical separations.

2.6.4 Multiple Controls

Simultaneous opposing commands may be transmitted through control circuitry in the tree.

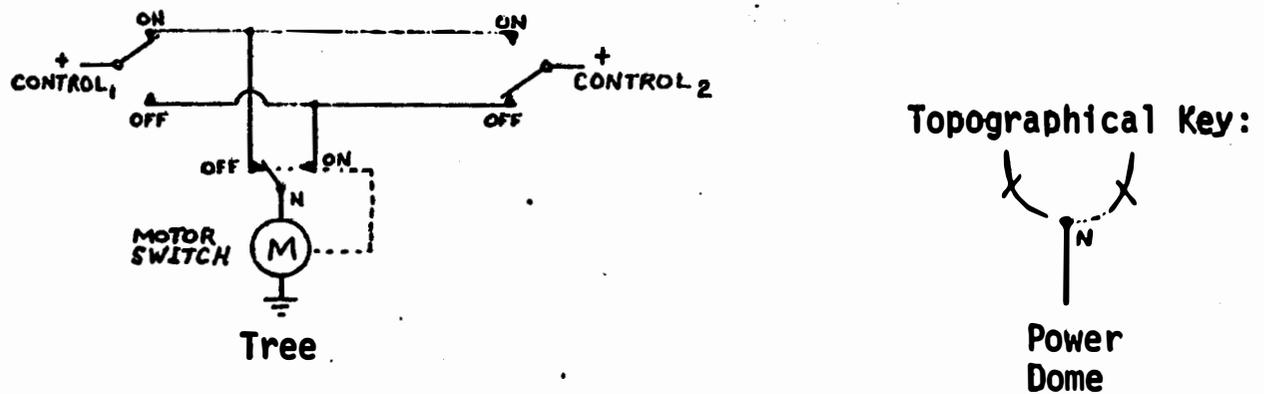


FIGURE 2-8 Multiple Control Sneak

The motor switch will cycle continuously for the switching modes shown. This is the result of too many independent controls allowing the possibility of bad timing in the switch operations.

2.6.5 Relay Race

Relay operation timing may generate incompatibilities. The illustrations given above consist of conducted current paths, but the influence of other links must be considered. For example, relay coils and their associated contacts will frequently be found in different trees, but the coil-to-contact relationship can be thought of as a "functional branch" relating the two trees. In fact, this is the approach used to find relay races and other bad timing results caused by the interaction of circuit elements that are not connected by hard wire. The functional relation between trees and the equivalent topographical representation are illustrated below.

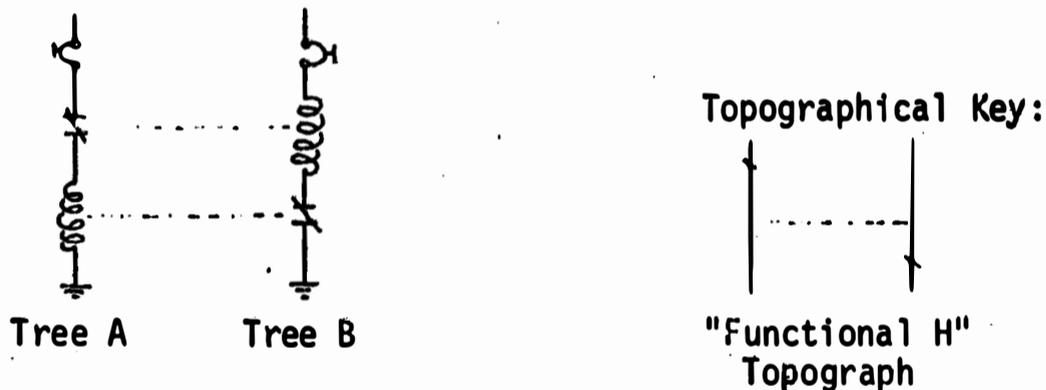


FIGURE 2-9. Relay Race Sneak

2.6.6 Ambiguous Indicators

Attempts to monitor multiple modes or functions with a single indicator endangers the fidelity of the status display.

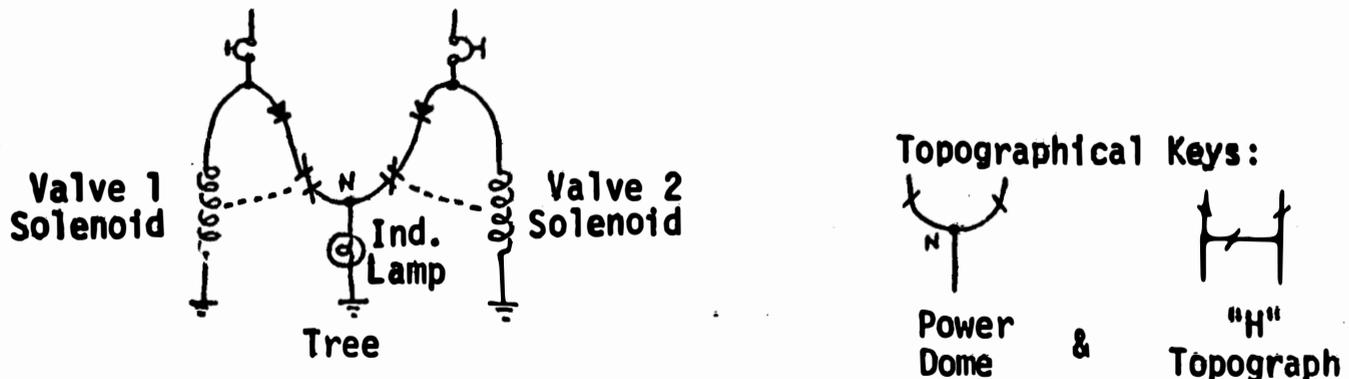


FIGURE 2-10. Ambiguous Indicator Sneak

The topographs and tree above show that either "switch" (solenoid contacts) can allow power flow through node N to ground. The tree illustrates that the lamp will indicate valve closure whenever either valve is closed. The lamp cannot conclusively indicate that both valves are closed.

2.6.7 Misleading Labels

Labels should denote all directly controlled functions for each switch, circuit breaker, and power source in the tree. Circuit breaker and switch labels in the areas of system interconnections are particularly prone to label discrepancies.

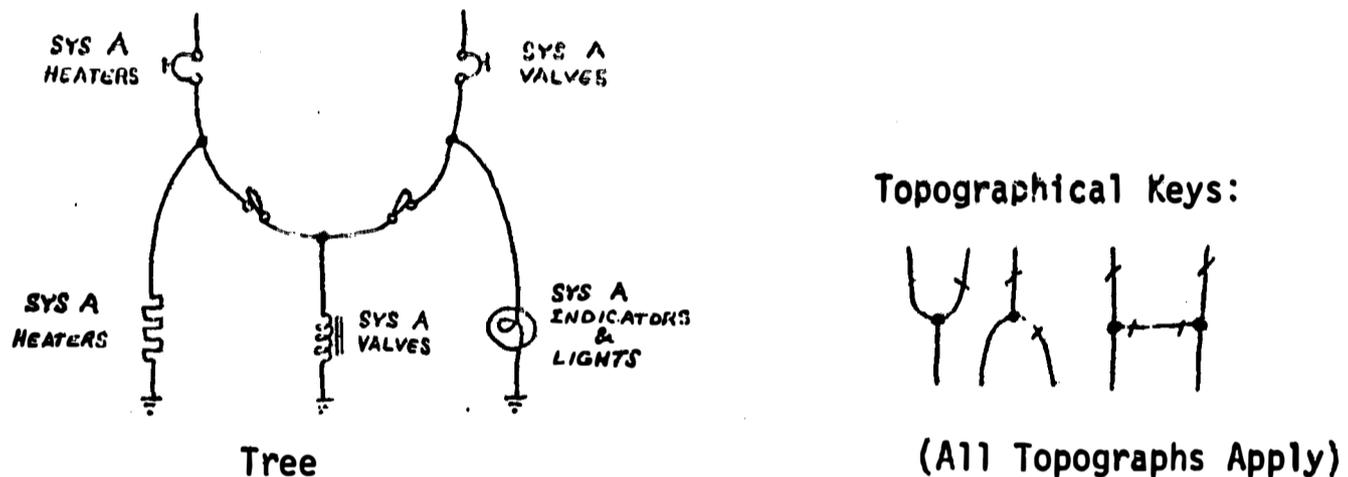


FIGURE 2-11. Misleading Label Sneak

The circuit breakers should be labelled "SYS A SERVICE" because each breaker can power the entire tree. In fact, the tree above should be analyzed for ambiguous indicators and reverse current flows.

The examples of sneak circuits presented in the above paragraphs do not attempt to illustrate all aspects of each of the clue types. Rather, commonly-encountered examples are given in order to establish an understanding of the clue patterns for each clue type. Specific clues and their most descriptive presentations can be developed for any particular type of system. However, all other such clue presentations should eventually resolve back to one or more of the four categories given earlier: sneak path, sneak timing, sneak indication or sneak label.

3.0 APPLICATION OF CONCEPTS

This section describes the tasks to be performed in a typical sneak circuit analysis of an electrical-electronic system. Data requirements, acquisition, filing and updating are described and emphasis is placed on the need for schematic accuracy. A technique for separating the overall system to be analyzed into parts of appropriate size and complexity is described. The construction of network trees using suitable symbols and the recognition of patterns and application of clues is discussed. Also, an operational computer program for searching through gross amounts of circuit interconnections to assist in the analysis is delineated. A major benefit from the use of this program is the efficient and accurate presentation of all circuit paths through the use of wire tape data from which the interconnect cables are fabricated.

3.1 Data

Of prime importance to the accuracy of a sneak circuit investigation of any system, regardless of complexity, is the exact knowledge of the electrical conductor continuities and the characteristics of electrical-electronic devices. Thus, the first task is to determine the requirements and establish the necessary agreements with the data suppliers to obtain and update all documentation.

3.1.1 Data Requirements

Electrical schematic and operational data is required for the analysis. This data may cross the broad spectrum of national and company security restrictions. If classified or proprietary data is needed, provisions for handling and maintaining these types of data must be supplied.

- a. Detailed Electrical Schematics: These internal black box schematics specify electrical component information such as the values of resistors, transistor code name, capacitor values, etc. These schematics are sometimes called by other terms and can be in book, sheet drawing, or microfilm form. These schematics are often required to complete the picture of system continuities.

- b. **Cable Interconnect Diagrams:** These diagrams define the black box interfaces and provide the representation of continuities between operating circuit elements. These cable wiring continuities in many advanced systems are represented by computer printout listings specifying "To" and "From" information by pin and plug in the wiring harness assemblies and are sometimes referred to as wire lists. Whatever the form, these data must describe each current-carrying conductor, node and terminal point and are usually authoritative sources of system cable continuity.
- c. **Integrated System Schematics:** System schematics usually take the form of an overall end-to-end drawing from power to ground and show the interconnect continuities for a certain function or subsystem. Within the particular black box only essential information is shown on this type of drawing. Information as detailed as (a) and (b) above may be included depending upon the circumstance. Notes and descriptive data are included to illustrate certain operating conditions such as principal mode, etc., to aid in system understanding. Due to a tendency to summarize for a specific purpose, the integrated type schematics that provide a reduced representation of a system may omit information vital to the identification of sneaks. Such things might be the omission of wires or plug and pin call-out and/or the use of equivalents instead of real circuits for such functions as amplifiers.
- d. **Design, Operating, Test, Training Manuals:** These and other documents describing the connection and operation of each system are utilized in sneak circuit analysis.

It must be recognized that the data available on any particular system will not correspond to the exact listing above, but equivalents to these data elements must be present. The picture of wire-to-wire continuities may require extraction from any or all of these data sources. Various methods of presenting detail component and system information must be surveyed in depth before proceeding into analysis because the data is the foundation on which a disciplined, effective sneak circuit analysis depends.

3.1.2 Data Control

Control of data to assure that the schematics reflect the actual equipment installed requires a permanent filing system set up in close proximity to the analysts. A constant flow of schematic and other pertinent data will take place between the file and the analyst. A filing system for recording incoming and outgoing drawings and documents is essential. Records of data source, number and changes are necessary. The same system must be set up for any microfilm cards. Close liaison must be established with the change control group so that electrical changes are immediately available. Changes in continuity will invalidate analysis conducted previously. For a data file which is being constantly changed, it might prove advantageous to use computer assistance which has proven capable of providing a permanent, quickly available, easily changed record system. Such a system was developed for the Apollo Program and might serve as a model. See section 3.6.1 of this document plus Reference 26, D2-118243-1 "Automated Filing Program Requirements" and Reference 27, D2-118209-1 "Automated Filing Program (AFP)".

Under the condition that more than one analyst is working in the same drawing area, it can prove advantageous to provide separate copies of integrated system schematics and operational manuals. However, control of storage and updating multiple copies adds to the data management problem.

During the analysis, data errors will be uncovered and communication with authorities responsible for data correction is necessary. Provisions for such vital communications should be established in the agreements for obtaining and updating data.

3.2 System Partitioning

This section points out some general guidelines in partitioning the total system so that analysis can proceed in an orderly manner. This is particularly required of large systems.

The finding of sneak circuits in any system is largely the

understanding of possible electrical continuities and switching conditions. In order to facilitate the analysis, the system may be divided as follows: upper power tree, primary power and control, secondary power and control, and signal circuits. These four tiers of operating circuitry are distinctly identifiable, and coverage of each is necessary because each may contain switching elements. Each tier is illustrated in Figure 3-1.

3.2.1 Upper Power Tree

The upper power tree consists of the power sources and the principal distributing elements to the main busses. This network does not include any loads but usually contains circuit interrupters such as contactors, circuit breakers, fuses, and switches.

3.2.2 Primary Power and Control

The primary power and control circuits distribute power from the main busses to primary loads. Thus the origin for this circuitry is the circuit protector (circuit breaker, fuse) immediately after the lowest bus in the upper power tree. These continuities extend from the circuit protector through interconnect wiring and controls, such as switches that vary the circuit continuities in response to operating conditions, through loads for return to the power source or ground. The primary side of transformers and the input to dc converters are loads included in this tier.

3.2.3 Secondary Power and Control

This tier of circuitry within a system contains elements that are deliberately isolated from primary power. All secondary power from transformers, dc converter outputs and associated circuitry are in this tier, with the exception of the signal circuits as defined in the next paragraph.

3.2.4 Signal Circuits

This final tier of system circuitry consists of continuities and other energy paths that are used for control display, recording and status. The signal tier of circuitry is considered necessary in the analysis because it contains switching and may cause sneak indications or have sneak labels.

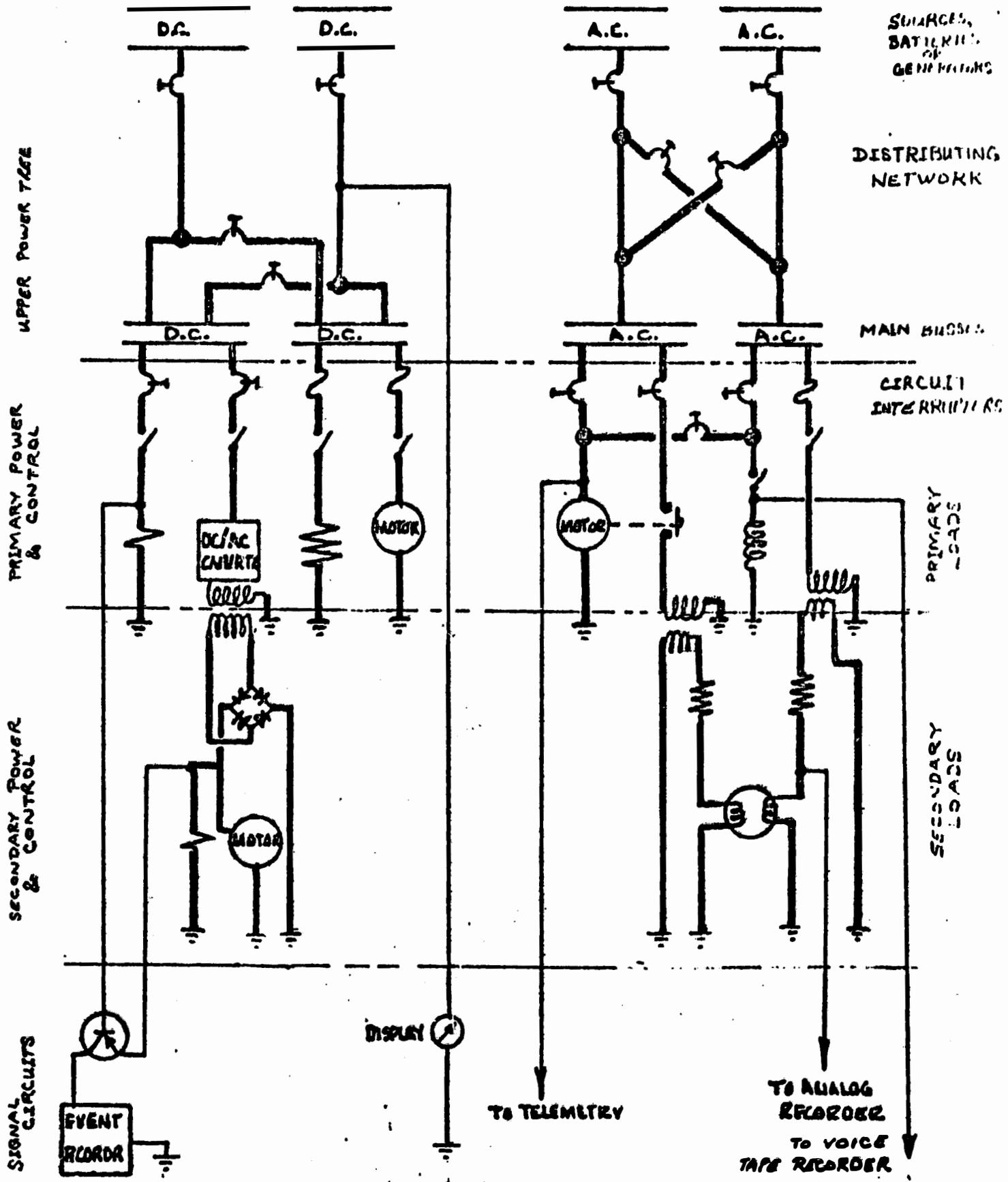


FIGURE 3-1. Example of System Partitioning.

Logic circuits which are synchronized with timing pulses are not included in sneak circuit analysis.

3.3 Network Trees

After the schematic data has been verified and a system of partitioning established, then the network trees can be constructed using selective loss of detail. Construction may begin on the upper power tree and at each circuit breaker controlling primary power. It also may begin at secondary power sources and switches controlling signal circuits. The goal is to diagram all possible circuit continuities, therefore switches are assumed closed in all positions. Standard symbology is used where possible and supplemented by simplified representations as necessary.

The network tree presents the continuities and components in a relative position to display the flow of power from top to bottom. The simple example below shows characteristic dendritic branching at nodes to distribute power to several lower busses or loads.

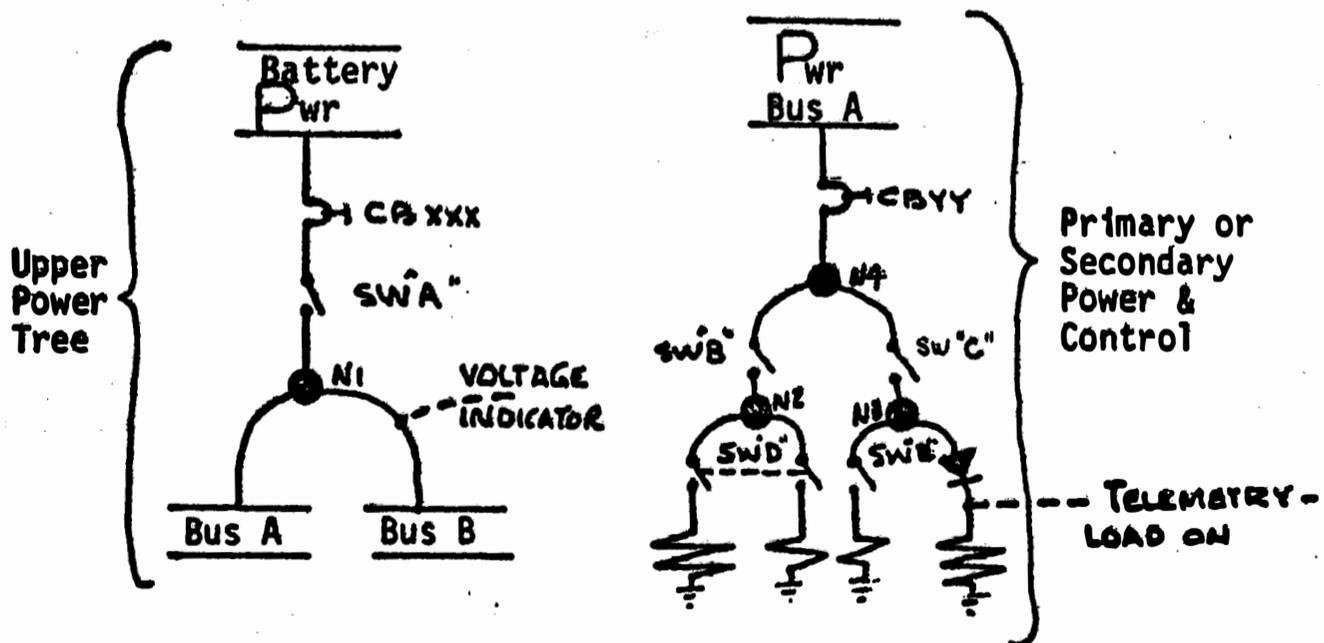
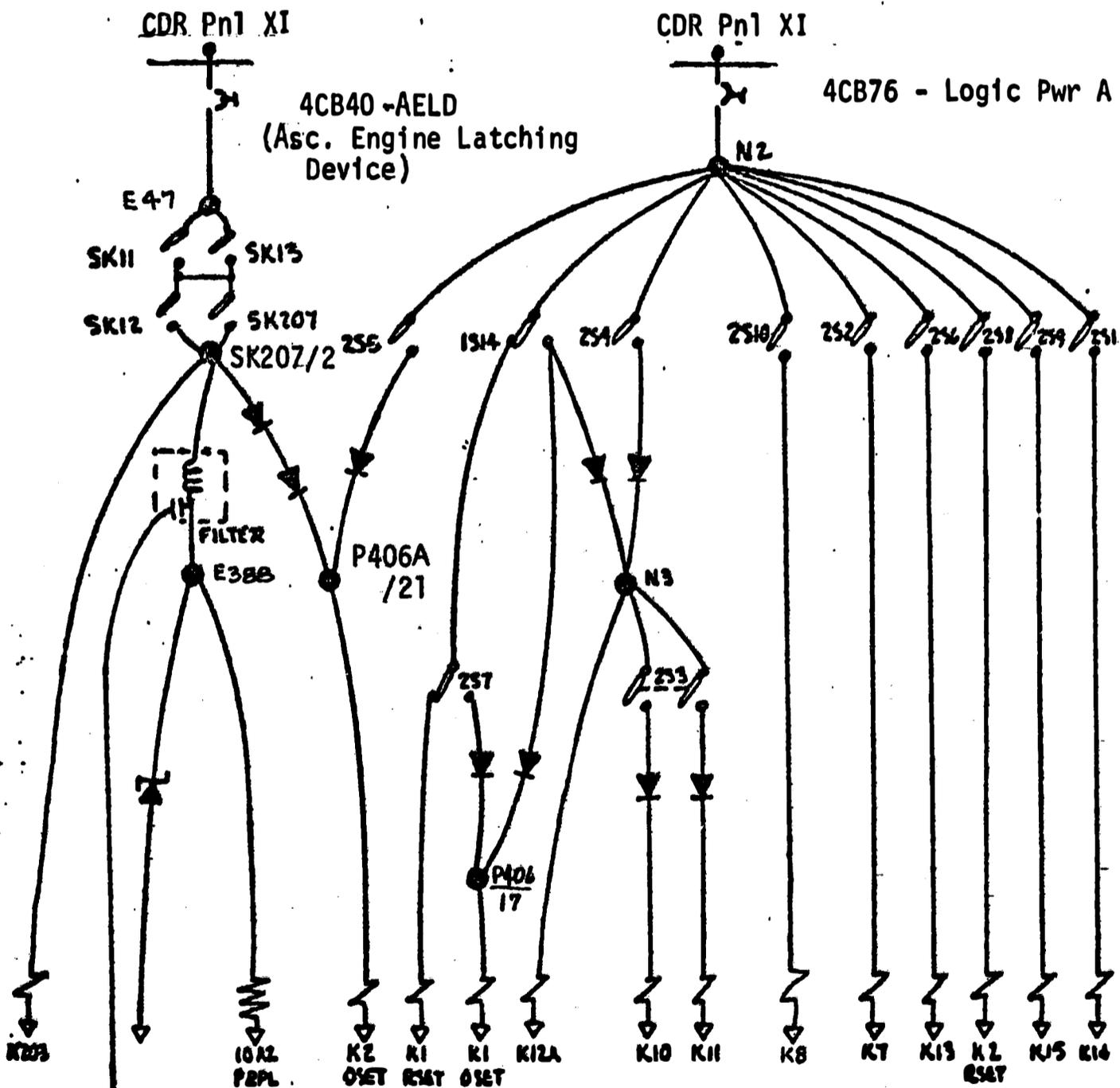


FIGURE 3-2. Elementary Trees

Placing all the continuity information on the tree will disclose each node, power, ground, load and mode control on one diagram. This diagram will display redundant circuitry, alternate power sources, and loads switched by multiple controls. A typical example is shown in Figure 3-3.



Switches

- 2S1 He Press Des Start.
- 2S2 He Press Rcs
- 2S3 ASC He Select
- 2S4 He Press ASC
- 2S5 Stage
- 2S6 Des Vent
- 2S7 Master Alarm
- 2S8 Stage Relay
- 2S9 Des Propel Isol Valve
- 2S10 Lndg Gear Deploy

FIGURE 3-3. Typical Tree

3.4 Tree Analysis

Certain patterns will be immediately evident from the network trees. However, knowledge of the function and operation of the circuitry is essential in the analysis of these patterns. This may be obtained from the integrated system schematics and operations manuals previously acquired in the data task. With this knowledge, power-to-power paths and paths permitting current reversal can be readily analyzed to assure proper circuit operation and timing. Power source or power bus isolation, if required, can be checked under all operational modes. The display of complete continuity assures that no latent connection can destroy the required isolation. Analysis of reverse-current branches will show any unintentional circuits that exist as a result of certain modes of operation, timing or lack of diode restriction on current flow. Application of the power-to-power and reverse-current clues is a first step in the analysis and is facilitated by the network tree topology.

After completing the analysis of suspect paths that are evidenced by the topology of the network tree, each node should be analyzed sequentially to assure complete investigation. In essence this requires checking each node to assure current flow in the required direction as dictated by the operations intended. The clues listed in the previous section should be applied in turn to determine that no sneak condition exists. This must be done for each mode of operation of the circuitry. One method of highlighting the various modes of operation of a given network tree is to make copies of the original tree and mark in the paths that are energized for each mode as shown below:

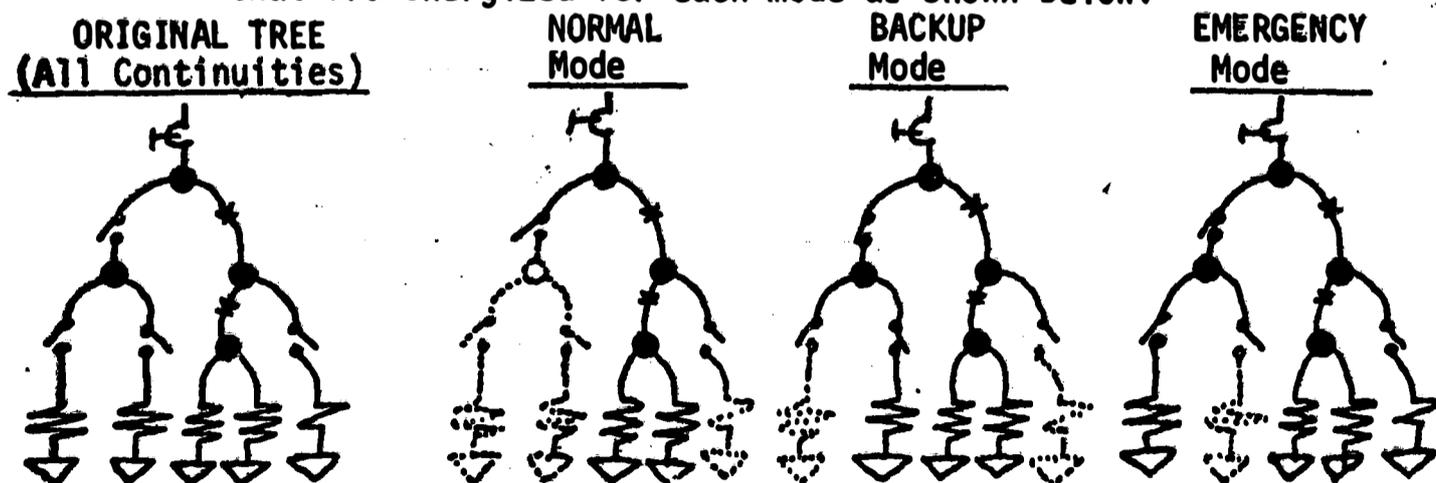


FIGURE 3-4. Mode Diagrams of Tree

A final step in the analysis is the investigation of interrelationships between network trees. This composite analysis requires thorough understanding of the functional aspects of the total system. Typical interrelationships are relay coil-to-contact, base-to-emitter control of transistor switches, gate control of logic elements, and motor switch controls. An example of interrelated network trees is shown below. Analysis of each of these trees depends on operations in another tree.

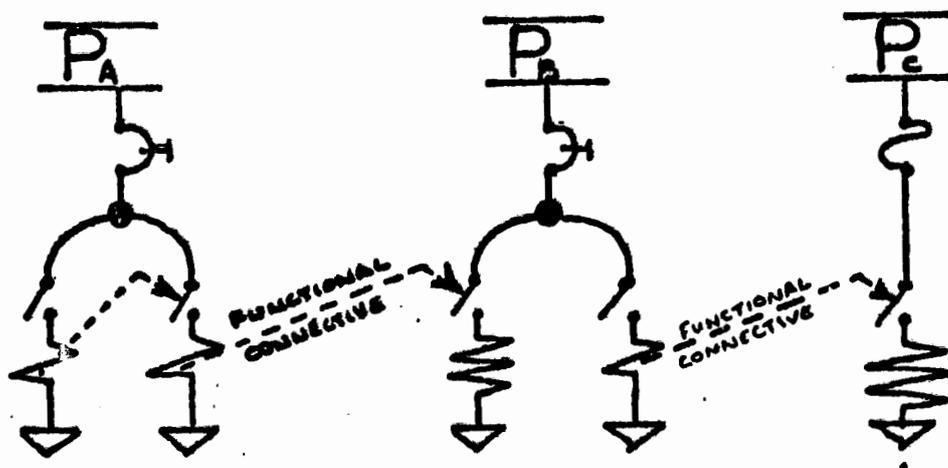


FIGURE 3-5. Interrelated Network Trees

3.5

Sneak Circuit Analysis Reporting

Two elements of sneak circuit analysis remain after the system has been analyzed in detail. They are the reporting of sneak circuits to the responsible authorities and the certification of analyzed circuitry as being free of sneak circuits. The network trees serve as a record of analyzed circuitry. A written report accompanied by a schematic diagram showing the sneak path or problem should be used to make affected parties aware of sneak circuits and of any required corrective action.

The sneak reports should be generated and properly dispositioned as each sneak circuit is discovered. It may also be desirable to conclude each major product, mission, or system with a summary report describing all the applicable findings of the sneak circuit analysis effort. The overall analysis and reporting may be assisted for large, complex electrical systems through data processing as discussed in the next section.

3.6 Computer Assistance in Sneak Circuit Analysis

Two computer programs have been developed to aid the Apollo sneak circuit analysis task. These are the Automated Filing Program (AFP) and the Automated Sneak Program (ASP). The Automated Filing Program is an information retrieval system which will store, sort, and report drawing index information. The Automated Sneak Program is a complex system involving a "pathfinder" program which traces circuit continuities to derive various reports used to assist engineering analysis. These two programs and their use will be discussed more fully in the following paragraphs.

3.6.1 Automated Filing Program (AFP)

The Automated Filing Program is used to establish the schematic baseline for the electrical analysis by effectivity-configuration listings. Drawing and schematic indexing details are input to AFP. A master file is then created from the drawing data. Upon user request, the master file information is sorted, and the required output will be printed. AFP will thereafter provide recall capability for other user requests. Complete details are given in D2-118243-1, "Automated Filing Program Requirements".

3.6.1.1 AFP Masterfile Information

The following information is contained in the AFP masterfile and is available in various formats for indexing the reference drawings to be found in the central drawing files:

- a. Reference designator of the component or subassembly
- b. Part number of the component or subassembly
- c. Schematic number
- d. Schematic title
- e. Vendor code (names supplier)
- f. Proprietary code (denotes classification)
- g. Released, but unincorporated, Engineering Orders (EO's) or Advance Drawing Change Notices (ADCN's)

- h. Subsystem codes
- i. File status (in file or not)
- j. Vehicle or end product effectivity
- k. Revision letter

3.6.1.2 AFP Reports

The above information can be sorted and reported by the computer in various formats. The three major sort routines are:

- a. Reference designator
- b. Part number
- c. Schematic number

In each case, a report can be provided for use in ascertaining file and schematic information. For example, if only the reference designator of a subassembly is known, the first sort and report routine given above will show all pertinent part numbers and schematic numbers. Likewise, if only a part number is known, the part number sort and report will list applicable schematics and reference designators. The schematic number sort and report gives all part numbers and reference designators associated with each schematic. Furthermore, these reports may be ordered by individual vehicle effectivities or by a range of effectivities, with the exception of the part number report, which is available by all effectivities only within the present program. Of course, in each report the applicable revision letters and outstanding Engineering Orders are given for each effectivity.

3.6.2 Automated Sneak Program (ASP)

The Automated Sneak Program is designed to remove engineering analysis dependency upon integrated system schematics. Integrated schematics inherently contain errors because they are humanly derived from the manufacturing information. Hardware production is based upon detail schematics and wire lists. These documents are more accurate, complete, and timely than the integrated schematics, which are generally produced when time is available and for engineering reference only. Even slight errors or change omissions in the integrated schematics can completely invalidate engineering analyses based upon those schematics. The alternative is use of detail schematics and wire lists for each engineering analysis. Usually, the volume of such information is so great that it discourages use by an engineer concerned with overall system knowledge. Moreover, such data is not in the format desired by electrical system analysts. The Automated Sneak Program provides a way of alleviating the menial task of tracing circuit continuities through detail schematics and wire lists. A general description of the program inputs, processes, and reports and their uses is given in following paragraphs. Complete details of the program operations are given in D2-118081-2B, "Requirements for the Automated Sneak Program," and in D2-118211-1, "Automated Sneak Program System Document."

3.6.2.1 ASP Inputs

The Automated Sneak Program processes circuit data from wire list tapes and from manually-prepared keypunch inputs which represent continuities within equipment modules and panels. The exact data and formats are discussed in D2-118081-2B, as referenced above. However, any discussion of the formats would be unique to Apollo and its multi-contractor environment; therefore, only the type of data processed will be discussed here. Appendix A illustrates Apollo input coding techniques.

The wire lists may already exist on computer tapes, or they may be generated from whatever production wiring records exist. The data must identify wire segments in terms of FROM and TO end points which are usually plugs, jacks, or

terminal boards. Of course, other end terminations are allowable. The basic idea is that the wire list will provide data necessary to describe circuit continuity between the external connectors on the equipment modules.

The equipment module internal data is supplied by converting the detail schematics into point-to-point continuities in the form of a manually-prepared "internal wire list," which is then keypunched for computer masterfile generation. FROM and TO end terminations are used to describe circuit continuity segments, which may be modified with functional and location remarks, diode and impedance notations, plus a variety of other information, as given in Appendix A of this document.

3.6.2.2 ASP Processes

The ASP system provides for updating the wire list masterfile and the equipment module continuity masterfile, as required in order to ensure accurate and timely circuit information. When the data masterfiles are complete (or at any other desired time), the program will merge the wire list with the equipment module data to provide total circuit continuity in one masterfile. The total data is then assigned numeric codes during a data reduction phase of the program and these numeric codes are strung together wherever continuity exists. In other words, the data is searched for complete numeric "circuit paths". Any incomplete circuits (open-ended wires) are also found and reported. After all the data has been searched, the resultant numeric circuit paths are regenerated back into the information carried on the wire list and equipment module masterfiles for ease of human interpretation and analysis.

3.6.2.3 ASP Reports

The regenerated circuit paths are reported in the ASP Path Report (See examples of all reports in D2-118081-2B). The Path Report shows the circuit continuity point-by-point with wire and equipment module identifications, pertinent drawing numbers, diode, impedance, and remarks information as originally input for each data segment. The naming convention of the points will identify switches, circuit breakers, relays, motors, and other such circuit components and loads. The Path Report therefore represents circuits in a listing form rather than pictorially, and also provides

reference information with functional remarks. Moreover, the Path Report forms the baseline for many derived reports to assist engineering analysis.

The reports derived from the paths are: Nodal Set Matrix, Terminal Branch Report, Switch Branch Report, Load Report, Diode Report, and Special Node Cross-Reference Report. These reports are discussed below, generally as a package composing a "Nodal Set," which completely describes a network tree.

a. Nodal Set Matrix

This report consists of a "connectivity array" which identifies the nodes in a network tree (related paths) and shows their relationship to one another within each path which forms the tree. Diode, switch, and load information is also contained. The report is used to sketch the network tree and provides "selective-suppression-of-detail" to simplify topological analysis.

b. Terminal Branch Report

This report lists the first and last branches (segments) of each path of the Nodal Set matrices. The information is used to label the power sources and ground points on each network tree. Open end points, which show unterminated wires or data discontinuities, are also given.

c. Switch Branch Report

This report lists all the circuit breakers, switches, and umbilical disconnects in each nodal set and references their respective paths. Each item carries its remarks and other information coded into the original input data. The report is used to compare functions of the switches within a tree and to label switch settings and functions on the tree sketch. It also calls attention to the fact that umbilical disconnects must be treated as switches in sneak circuit analysis because they are uncoupled during the anticipated system operation.

d. Load Report

This ASP report lists all the items within a nodal set

that are coded in the original input data as circuit loads ("L" - item names). It is used to draw and label pertinent loads on the network tree sketch. A remark will identify the function of each load.

e. Diode Report

This report lists the diodes and their respective paths within each nodal set. It is used to draw and label all diodes on the network tree. The input remarks will provide any special information regarding each diode.

f. Special Node Cross-Reference Report

This ASP report provides a functional cross-reference for specially-coded items within each nodal set. For example, K1 may represent a relay coil in Nodal Set 003. The Special Node Cross-Reference Report for Nodal Set 003 will then show the nodal set identification of contacts controlled by K1. Multiple relationships are allowed, and the cross-reference is given for each special node -- i.e., both for the coil and for the contacts in their respective nodal sets. Of course, the cross-reference technique is applied to many uses in addition to relay coils and contacts.

3.6.2.4 ASP Tree-Sketching Procedure

The ASP reports are used per the following procedures to completely sketch and label the network trees:

a. Sketch the Tree

Use the Matrix, Terminal Branch Report, Switch Report, Load Report, and Diode Report. It is suggested that a rough draft of the tree be made from the matrix, then redrawn for better layout before labeling the tree. Sub-tree cross connections through high impedance may be shown as opens with notation of impedance and references between sub-trees when more than one page is required.



FIGURE 3-6. High Impedance Sub-Tree Partitions

b. Add Labels to Tree

Identify nodes, power sources, grounds, switches, loads, and diodes. Use the Terminal Branch Report, Switch Report, Load Report, and Diode Report as required. Any "special" nodes or points (I, SI; K, SK item types) found in the paths should be shown on the tree and cross-referenced to their associated special nodes by using the Special Node Cross-Reference Report.

- 1) Umbilicals and Stage Breaks must be shown as an X on the tree. Use the Switch Report.

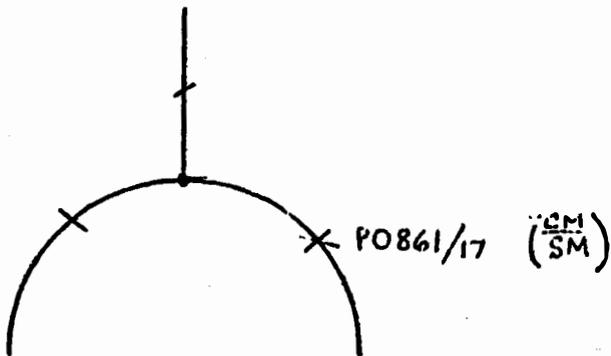


FIGURE 3-7. Umbilicals on Tree

- 2) Loads and Diodes will be identified from the Load Report and the Diode Report. Label the items on the tree. The sketch should reflect the type of load per Figure 3-8.

- 3) Switches should have both pins shown to indicate positions. Functional labels must be shown.
 - 4) Notes should be written to explain the circuit function and provide other information to aid analysis.
 - 5) Titles should be used on each sketch to identify the network.
- c. Verify the Tree against integrated and detail schematics where necessary.
- 1) Make any necessary data corrections on the tree and in the computer data masterfile.
 - 2) Yellow-line the areas of the integrated schematic master copy that are represented by the tree. This will provide a check on circuit coverage and discover drawing errors or data discrepancies.
- d. Show the Operational Modes of the tree configuration by copying the original tree and drawing the switches in their proper position for each function on a separate copy. Title each copy to define the operational function. DO NOT ATTEMPT TO SHOW ALL SWITCH PERMUTATIONS OF THE TREE. An extra copy of the original tree should be made for future use and filing.

After the tree is completely drawn and labelled, analysis for sneak circuits proceeds as discussed earlier in Section 3.4 of this document.

3.6.2.5 Additional ASP Capabilities

The Automated Sneak Program in its present state assists sneak circuit analysis. It also serves as a data source and baseline for various special tasks. In addition, it can provide a foundation for many developments in the field of computer applications to engineering endeavors. Some of these areas are discussed in the following paragraphs.

The data masterfiles of the Automated Sneak Program are useful data for sorts to determine and list such things

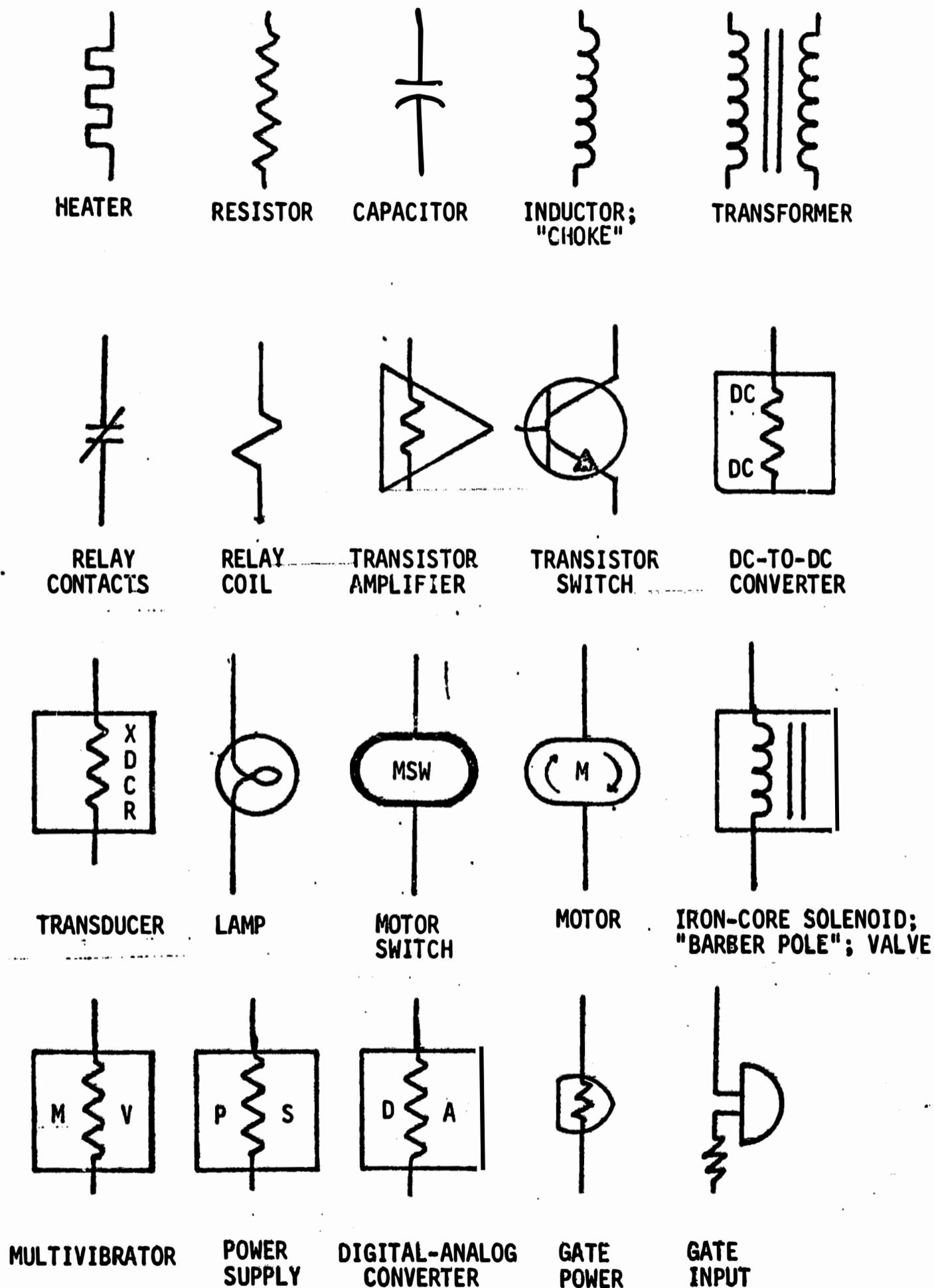


FIGURE 3-8. Load Symbols for Tree Sketches

as all circuit breakers with their ratings, functions, locations, and applicable schematics. Such a sort can easily be produced for switches, umbilicals, loads of various types, diodes, monitor points, etc. The listing can also include a reference to the pertinent network tree by nodal set number.

Engineering analyses other than sneak circuits can use the network tree sketches produced through ASP. Battery and bus loading studies, Failure Mode Effects Analysis, wire sizing studies, anomaly and change analysis, and other engineering tasks can use the trees to gain quick system knowledge, then supplement the trees with the paths and other reports for access to specific details and location of applicable schematics. Indexes are produced to enable speedy location of any circuit item in its ASP tree, and from there, related information may be obtained through ASP data.

An area that should be pursued within ASP is that of providing "change package" capability wherein only differences are reported within trees produced by successive ASP runs. (In fact, such a program requirement specification has been prepared in Houston: inter-department coordination sheet 5-2933-HOU-065-014, "Nodal Set Comparison Program"). Even better would be a capability to run the program to process only changed data and report accordingly. (A "crutch" method of performing that function is now available through selective circuit searches, but this presupposes that the changed areas are known.)

Within present state-of-the-art is the capability to use data produced by ASP to generate network trees drawn on microfilm/CRT plotters by a computer. Such trees can eliminate the manual sketching task now required to utilize ASP output. The computer-produced trees can be expanded to various levels of detail and replace or supplement existing integrated schematics. The same technique could lead to automated detail schematics, with engineering information released entirely through data processing.

Perhaps the ultimate machine utilization in engineering tasks will come with interactive graphics whereby an on-line CRT terminal is used to display the trees at a continuously

variable selective level of detail to supply the greatest assistance in network analysis. Such a terminal could also be used for real-time change input, analysis, approval, and release. It would provide instantaneous data availability and correction capability, and feedback channels could be included from all users in the production environment. A system of such terminals could then evolve into a replacement for existing techniques of engineering communication on paper through drawings. The CRT display terminal system would offer inherent advantages in data availability, quicker reaction time for changes, and space/weight savings over the existing drawing systems of communication.

Summary and Conclusions

Figure 3-9 shows the steps involved in performing a sneak circuit analysis. The flow diagram is generalized, and the conversion of data to continuities, etc., is necessary for the purely manual or the computer-assisted approach. The differences arise in formats, techniques, and orderliness of record keeping. The automated method offers other advantages over the manual approach. These are:

- a. Removes dependency upon "derived" system schematics, which may not be "as built"
- b. Provides different perspective, forcing analyst to see circuitry different from designer's viewpoint
- c. Traces detail continuity faster than manual, without tiring or overlapping areas
- d. Forms general data base for other engineering uses
- e. Offers development capabilities for new applications and processes

Disadvantages of automation are:

- a. Data processing equipment requirements
- b. Learning curve for techniques and operating knowledge of program operations
- c. Batch processes at present, rather than quick, selective response offered by on-line systems

Sneak circuit analysis has been found to be expensive, but worthwhile. One sneak occurrence can cost more than the entire analysis. Ideally, the analysis should be performed as soon as complete design details are known, and it should be conducted by a team independent from the design organization to avoid prejudice in system reliability. In any event, the analysis must be performed by personnel with total system overview capability, for it is the subsystem or assembly interconnections which most frequently give rise to sneak probabilities. Each component and assembly is usually adequately designed and tested to do its job in a fixed environment, but as the total system size and complexity grows, so does the capability of the anticipated environment to change unexpectedly.

Sneak circuit analysis offers an approach to more completely determine all possible system modes, both the expected and the unexpected. Therefore, sneak circuit analysis can help reduce system costs by preventing unexpected equipment damage during test plus subsequent redesign and retest. Moreover, sneak circuit analysis can help achieve a more "failsafe" product through complete evaluation of all system responses which may be brought about by procedural discrepancies. Finally, through the various levels of overview provided by the selective-loss-of-detail approach in sneak circuit analysis coupled with automated display devices, new dimensions in engineering capability may arise to successfully design and integrate ever larger complex systems.

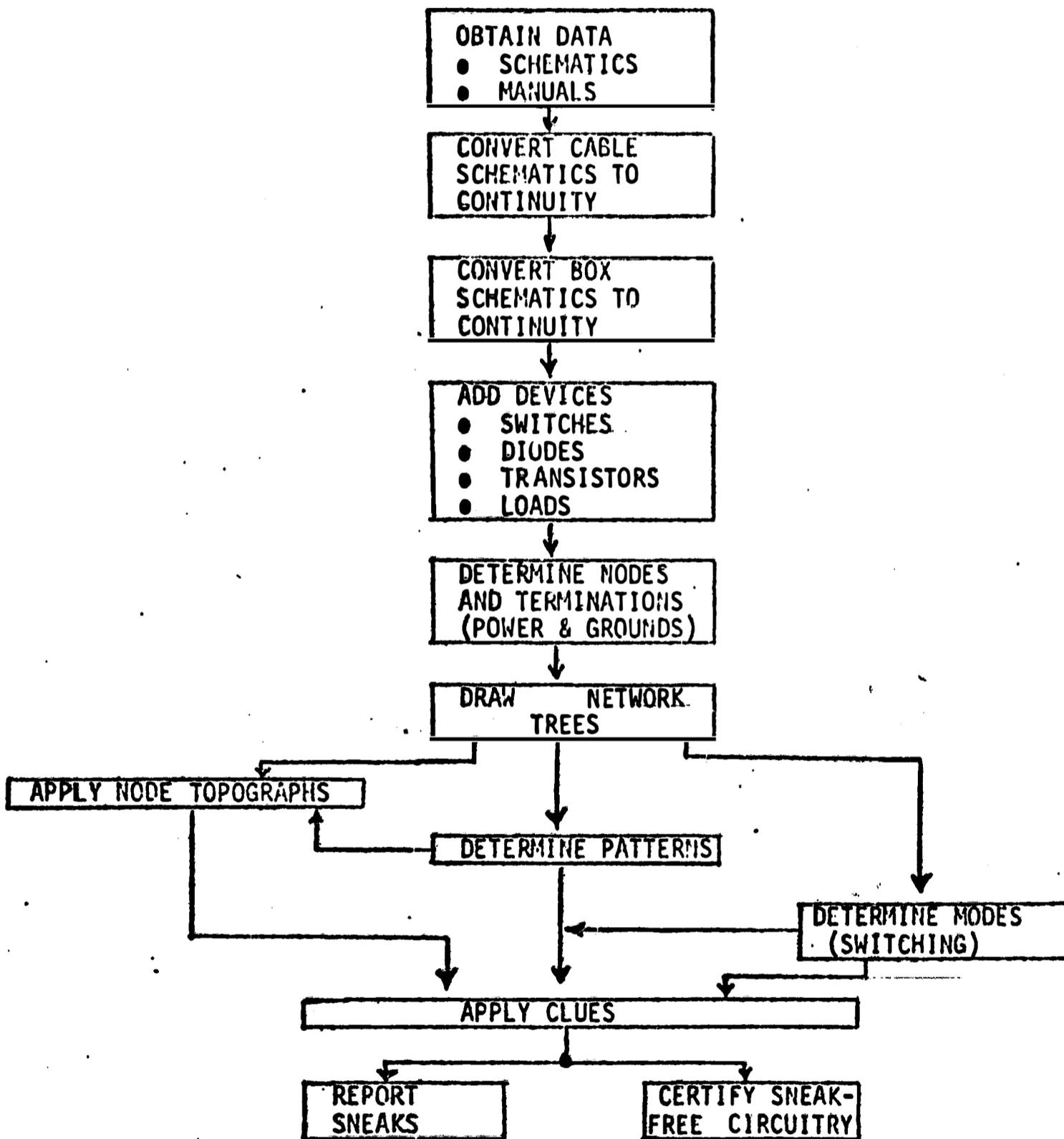


FIGURE 3-9. Sneak Circuit Analysis Work Flow Diagram

APPENDIX A

APOLLO BID INPUT GUIDELINES

This appendix illustrates basic guidelines for the Apollo Automated Sneak Program "black box" internal data (BID) coding.

A.1 Card Type and Format

There are two types of BID input. The B1 input provides general information about a particular "black box", whereas each B2 input describes a continuity segment within the box, equipment module, or panel.

a) B1 Input Format, Figure A-1

Every B1 input will be composed of fields containing the following information:

Control Field

- 1) B1 identification code, col. 1-2
- 2) action code, col. 3
- 3) reference designator or model number, col. 4-18

Non-Control Data

- 4) contractor code, col. 19
- 5) area code, col. 20
- 6) bay number, col. 21-23
- 7) drawing number, col. 24-41
- 8) part number, col. 42-61
- 9) box title, col. 62-80

The control field is that portion of the data necessary for the record to be unique and is generally used in sorting. The information outside the control field of a record is considered reference data.

After a B1 record for a particular black box is on file, it will be possible to describe the internal wiring of the box with B2 inputs.

b) B2 Format, Figure A-1

The second type of BID input, B2, describes the internal wiring of the black box. Every B2 input will be composed of fields containing the following information:

A.1 Continued

Control Field

- 1) B2 identification code, col. 1-2
- 2) action code, col. 3
- 3) reference designator or model number, col. 4-18
- 4) From designation composed of From item col. 19-24, and From pin, col. 25-28
- 5) To designation composed of To item, col. 29-34, and To pin, col. 35-38

Non-Control Data

- 6) diode, col. 39
- 7) impedance, col. 40-42
- 8) remarks, col. 43-80

A.2 Action Codes

The computer will perform one of three possible actions with each input. The allowed action codes are "A", "D" and "R". An "A" code instructs the computer to add the input to the data file. A "D" code instructs the computer to delete data from the file, and an "R" code instructs the computer to revise information beyond the control field of the record, which must already be on file.

A delete action code on a B1 input card will cause all records on file for the box to be deleted -- the B1 plus all the related B2 records will be removed from the computer masterfile. However, a delete action code on a B2 input card will cause only the corresponding B2 record in the computer masterfile to be deleted. Thus, if an entire box needs reworked, a BID card can be submitted to remove all the old data, and a new set of B1A and B2A cards may be included in the same run to re-establish the box in the desired configuration on the computer masterfile. When only a few segments need reworked, the individual B2D and B2A inputs may be used without disturbing the remainder of the box records.

When it is not necessary to eliminate a continuity segment specified by a given From-To pair but it is desired to change the diode polarity, impedance value, or remarks for the segment, then the revise action code (R) should be used. With "R" in column 3, the computer will replace the applicable field with the new data entered on the card. A complete control field is required to identify the appropriate masterfile record, of course. Thus, if the masterfile has a record

(OLD MASTERFILE RECORD)

B2 C15-4A404 P0215 0003 J0017 00A1 + 001 PWR TO J-BOX

A.2 Continued

and an update card as follows is submitted,

(UPDATE CARD)
B2R C15-4A404 P0215 0003 J0017 00A1 999

then the revised masterfile record will be

(NEW MASTERFILE RECORD)
B2 C15-4A404 P0215 0003 J0017 00A1 + 999 PWR TO J-BOX

Notice that the diode polarity (+) and the remarks (PWR TO J-BOX) were not changed in the above example because the update card indicated no revision to those fields. Another example will further illustrate how the revision code works:

OLD MASTERFILE RECORD:

B2 C15-4A404 P0215 0003 J0017 00A1 + 999 PWR TO J-BOX

UPDATE CARD:

B2 C15-4A404 P0215 0003 J0017 00A1 @ GND

NEW MASTERFILE RECORD:

B2 C15-4A404 P0215 0003 J0017 00A1 999 GND

In the above update, the commercial "at" (@) was used to revise a field to blank. In fact, the commercial "at" in the first column of a non-control field on a revise update card will cause that entire field to be replaced with blanks, regardless of whatever else may be shown in the field on the update card. The example also illustrated a remarks field revision. Since updating is done by fields on revisions, whatever is shown on the update card (except blanks, of course) will entirely replace the corresponding field on the masterfile.

A final note on revisions -- the "R" action code will not affect data within the control field. The control field is used on the update card so that the computer can match the data on the masterfile tapes, thus identifying the record to be changed in the masterfile. Therefore an update card consisting of

B2R C15-4A404 P0215 0003 J0017 00A1

would cause no change on the masterfile. The computer would find the corresponding old masterfile record, then write it out again on the new masterfile tape with no change, since no revisions were indicated in the non-control field areas. Also, keep in mind that

A.2 Continued

the revision code works the same way, by fields, on B1 inputs. The only difference is that the B1 control field is shorter than that of a B2, and the non-control fields contain different data. Again, every BID input card must contain a card type (B1 or B2), an action code (A, D, or R), and a box reference designator (to identify the box name).

A.3 Contractor and Area Codes (B1 Only)

Contractor and area codes are required on every B1A card. However, because they are not in the control field the codes are not required on B1R or B1D inputs. The contractor code identifies the hardware prime contractor. The codes in use for Apollo are:

- N - North American Rockwell
- G - Grumman Aircraft Corporation
- A - AC Electronics Division

Area codes specify the general location of the equipment in the spacecraft. The Apollo codes in use are:

- A - Spacecraft/Launch Vehicle Adapter
- C - Command Module
- E - Launch Escape Tower
- G - Ground Support Equipment
- L - Lunar Module
- S - Service Module

A.4 From and To Terminations

The Automated Sneak Program determines paths of electrical continuity by connecting circuit segments through common end points. B2 inputs define circuit segments within a black box in terms of continuity "From" one point "To" another. When the continuity segments of a box reach the external interfaces, the path is continued through data supplied by the wire lists, which are also in terms of From and To designations. Therefore, particularly at the external interface connections of each box, coding conventions are required to enable circuits to be followed from the boxes into the wire harnesses. Other coding conventions have been established to provide for summary report production and special processing. These coding conventions are discussed in the following paragraphs.

A.4.1 Equipment Connectors

Plugs and jacks are generally used to connect black boxes to the wire harnesses. Therefore, the path tracing program will pass from a box connector in the BID masterfile to a wire list connector of the same name so long as the contractor and area codes match. For this reason it is required that the BID continuity segments be coded to the external harness connector rather than to the unit connector which is a part of the box. Likewise, the harness connector must be identified in the BID exactly as it appears in the wire list.

Plugs and jacks in the wire list will be defined with a "P" or "J" character in the first column immediately followed by four numerics and possibly another alphabetic character. Also, pin designations always consist of four characters right-justified with leading zeros. With this in mind, if an equipment detail schematic shows an external connection to harness connector P21 pin J, then the appropriate BID input would identify the connection as P0021 pin 000J, and this would agree with the wire list data. In other words, P21 pin J is not equal to P0021 pin 000J in the computer. Strict adherence to this convention is required wherever the BID must mate with the wire list through plugs and jacks.

There are instances in which the BID must be mated with the wire list through items other than plugs and jacks. To allow for such cases, the computer program will mate box data with wire list data for all identical items (with matching contractor and area codes) except the following:

- a. SXXXXX -- switch designations
- b. EXXXXX -- splice designations
- c. NXXXXX -- node or point names
- d. TBXXXX -- terminal boards
- e. CBXXXX -- circuit breakers
- f. [special character]XXXXX --- arbitrarily created reference points

where X = any character

and special characters are: %,), *, (, +, -, ., /, @, \$, =, numerics, and , (comma).

Items named with any of the above list of exceptions remain unique within each box and separate from any similar item in the wire list. Thus, there can be an S0001 in box C14A1, an S0001 in box C15-4A404, and an S0001 in the wire list; and each will remain separate from the others during the path trace. In other words, each of the above will be recognized as a unique point by the computer, whereas a point coded C14A16 in the BID

A.4.1 Continued

will be taken to be identical to a point named C14A16 in the wire list. Of course, pin data is also matched for every item before uniqueness or equivalence is determined.

A.4.2 Splices and Nodes

Internal splices and arbitrarily-named nodes will be coded with "E" only if the detail schematic has identified points on the drawing with such names. The "N" code is commonly used when assigning a name to an otherwise unlabelled junction of lines in the drawing. The use of arbitrary "E" and "N" codes should be minimized for ease of subsequent reference from computer paths to integrated schematics, wherein the "E" and "N" items will not be found. Frequently an unlabelled junction of lines on a drawing can be named as one of the items to which it connects -- i.e., the length of a line without impedance, etc., can be shortened to zero.

A.4.3 Terminal Boards and Circuit Breakers

Internal terminal board connections should be coded in the BID exactly as shown on the detail schematics. It will, however, be necessary to create From-To continuities for the bussed pin connections. Otherwise, each internal terminal board pin will remain isolated from all other pins of the terminal board.

Circuit breakers within a panel should be named as given on the detail schematic, so long as the "CB" codes are entered in the first two columns of the item field. It will be necessary to enter each pin of the breaker, along with their connected items, and then to create a segment between the pins. Thus, to completely specify continuity through a circuit breaker, the From-To segments would be:

<u>From</u>	<u>To</u>
Point X	CB5-0001
CB5-0002	CB5-0001
CB5-0002	Point Y

A.4.4 Switches and Fuses

The computer will treat as a switch any segment with identical From and To items (and different pins) that begin with the letter "S". Thus, many types of switches can be specified by using "S" plus other conventions for the remainder of the item name. For

A.4.4 Continued

example, S-numeric is generally accepted as a manual switch in the Apollo data base, whereas SQ-numeric denotes a transistor switch. Likewise, "SK" (followed by numerics) is used for relay contacts, "SLV" for valves, "SCR" for silicon-controlled rectifiers, "SM" for motor switches, and so forth.

As was the case for circuit breakers, continuity segments must be supplied between the pins of a switch. Thus, for a simple single-pole, single-throw switch the continuity would be:

<u>From</u>	<u>To</u>
Point A	S1-0001
S1-0002	S1-0001
S1-0002	Point B

For slightly more complex switch, such as the shorting switch illustrated in Figure A-2, the continuity would be:

<u>From</u>	<u>To</u>
Point C	S2-0001
S2-0002	S2-0001
S2-0002	Point D
S2-0001	S2-0003
Point E	S2-0003
S2-0001	S2-0004
Point F	S2-0004
S2-0002	S2-0003
S2-0003	S2-0004

where the last two segments denote the shorting feature of the switch.

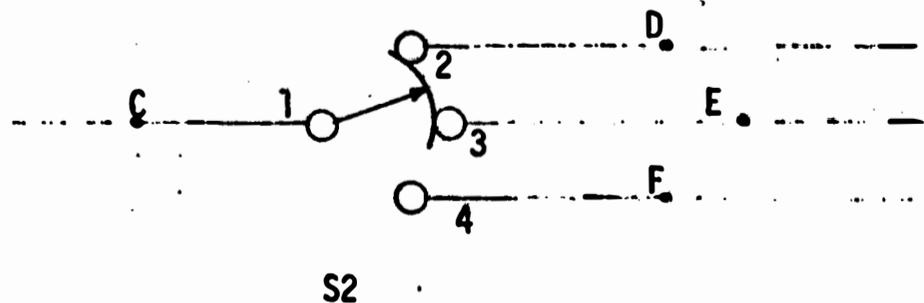


Figure A-2. Illustration of Shorting Switch

A.4.4 Continued

Multiple-pole, multi-throw ganged switches, as illustrated in Figure A-3, can be coded to denote each throw:

<u>From</u>	<u>To</u>
Point G	S3-0001
S3-02T1	S3-0001
S3-02T1	Point I
S3-0001	S3-03T2
Point J	S3-03T2
Point H	S3-0004
S3-05T1	S3-0004
S3-05T1	Point K
S3-0004	S3-06T2
Point L	S3-06T2

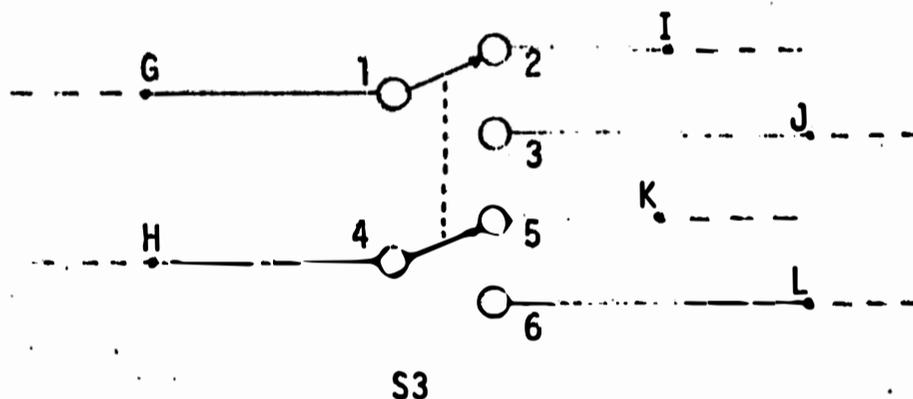


Figure A-3. Double-Pole, Double-Throw Ganged Switch

In the above coding the "throws" are arbitrarily numbered as 1 and 2. The letter "T" in the pin field denotes the throw number (position), and the first two digits of the pin field are used to specify the actual pin number. Such coding will allow recognition of the nature of the switch in the computer reports and will facilitate subsequent analysis of the network trees with respect to switching modes.

Fuses will also be coded as switches because they may "open" a circuit, and the tree must be analyzed for such a situation. Therefore, the code "SF" is reserved for fuses, and the continuity must be specified in terms of pin numbers which create a "switch branch":

A.4.4 Continued

<u>From</u>	<u>To</u>
Point M	SF15-0001
SF15-0002	SF15-0001
SF15-0002	Point N

The pin numbers must be supplied and may be arbitrarily assigned if none are given on the detail schematic.

A.4.5 Loads and Relay Coils

Circuit loads other than biasing resistors and the like are to be coded with the character "L" for the From item of the segment containing the load. For example, the codes

<u>From</u>	<u>To</u>
Point P	L1
L1	Point Q

might be used for the example of Figure A-4.



Figure A-4. Load Coding Example

Various categories of loads can be specified through the establishment of additional coding conventions as was done for switches. Thus, "LM" denotes a motor, "LH" denotes a heater, "LTF" denotes transformers, and so forth. The remainder of the item and pin fields can be used to specify uniqueness within each box.

Relay coils are loads which receive a special code, "K", for a special purpose. The use of this code allows the computer to report the relationship between a coil and its contacts, even though they may be in different paths and trees. This is accomplished through matching K-items with SK-items in the same box. A match will occur if the K-item is identical to the SK-item without the "S". Pins are not compared, nor is the last character of the K-item field, which may thus be used to specify uniqueness of several coils related to the same set of contacts. The K-item must be identified relative to the segment containing the coil just as was done for other loads.

A.4.6 Special Nodes

In addition to the special purpose coding of "K" and "SK" items discussed above, another set of codes have been reserved for a similar purpose wherever desired. These codes are "I" and "SI", and they may be used to define a relationship between any two elements, paths, or trees. There are some differences, however. The SK-items were always coded as switches, whereas the SI-item need not represent a switch. Moreover, the comparison of "I" to "SI" terminations will include the pin fields of each. That is, the pins must be identical to obtain a match and cross-relation. However, the last character of the I-item is still not compared and may be used to provide uniqueness so that several I-terminations can be related to a single SI-termination.

A.4.7 Power and Ground

Power and ground points are to be coded as "PWR" and "GND", respectively. The pin fields may be used, if desired, to indicate levels or types of each condition. The computer will begin tracing continuities from each PWR point unless the point terminated a previously-traced path. It will stop any given path upon reaching a GND point.

Levels of power and ground are discussed in Section 3.2, System Partitioning, of this document. Pin 0001 is used for the upper power tree (distribution circuitry), pin 0002 for the primary power and control circuitry (direct loads), pin 0003 for secondary power and control circuitry (isolated loads), and pin 0004 for signal circuitry (control monitoring).

Generally, the location of the point labelled GND in the BID should be as far up into the tree as possible from the actual grounds without crossing a switch, diode, load, or other circuit element. In other words, the GND label should be used at the first-encountered constant zero potential or voltage reference point, looking down from the power source. This technique will prevent all the network trees from being tied together in the data through the ground return circuitry. If this were allowed to occur, then all the trees would be reported as one by the computer. Actually, the ground-pushing technique is another form of system partitioning, and the ground circuitry can be separately coded with its own "PWR" points so that the "ground tree" is reported for separate analysis.

A.4.8 Parallel Branches

Parallel branches between nodes call for special handling. The computer sorts uniquely on the From-To pair within a box. Therefore, there can be only one of any particular From-To pair per box. That is, only one branch can be directly specified between any two points. There are, of course, work-around techniques to overcome the situation. First, parallel branches should be represented by a single equivalent branch wherever possible without loss of circuit features. For example, a single load to ground may be input with a coded remark that the load "occurs 10 times".

If the equivalency approach is not desired, then dummy data points may be introduced into the parallel branches to establish unique branch records for the computer. An example is given in Figure A-5.

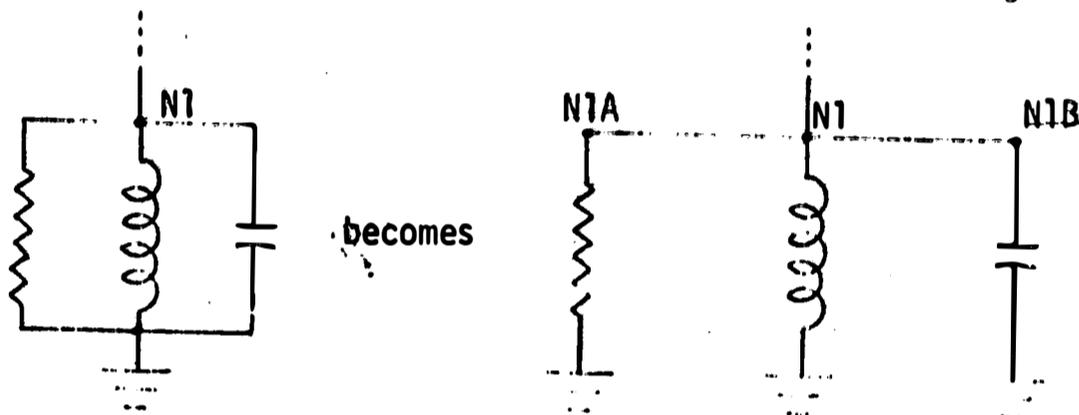


Figure A-5. Coding of Parallel Branches

In the above example N1 could not have been coded directly to ground for each of the three branches. By introducing the dummy data points N1A and N1B, each point (N1, N1A, and N1B) can be coded to ground as a unique branch, and N1 can be coded to N1A and N1B through unique dummy branches. The computer programs will later eliminate the dummy points from the network tree data, so that the tree will show only N1, with three branches to ground.

A.5 Diodes

The presence of diodes in a circuit segment will be indicated by coding "+" or "-" in column 39, depending upon the diode polarity. If the diode allows current flow from the From item to the To item, then the "+" will be used. Reverse polarity (from To to From) is indicated with a "-". Generally, diode indications should be given for unidirectional circuit components, such as transistor switches and SCR's. The diode indication in these cases is to be given within the switch branch.

A.5 Continued

Zeners can be shown as normal blocking diodes with a remark to denote the type of diode and its breakdown voltage. A special convention has been established for arc-suppression diodes. Rather than create a dummy point to code the parallel branch containing the arc-suppression diode, the presence of the diode can be indicated by placing "DIOD" in the pin field of the item given on the high side of the suppressed coil. If other pin call-out requirements exist, "D" in the first column of the pin field will be sufficient. It is then understood that a parallel branch exists with a diode facing into the item carrying the "D" in the pin field. Figure A-6 illustrates an arc-suppressed relay coil.

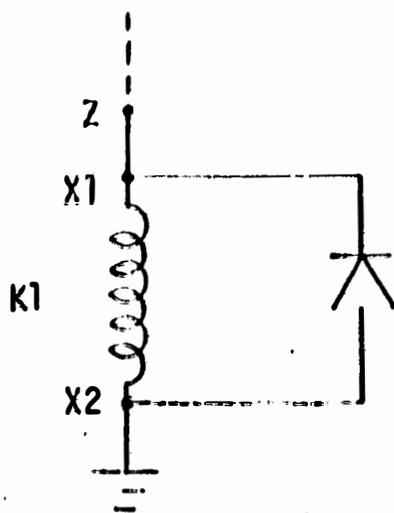


Figure A-6. Arc-Suppressed Relay Coil

The coding for the example of Figure A-6 would be:

<u>From</u>	<u>To</u>	<u>Diode</u>
Point Z	K1-DOX1	{blank}
GND	K1-DOX1	{blank}

The diode field is not also used to indicate arc-suppression diodes so that the field remains available for blocking diodes which may be placed in series with the coil. This coding technique additionally serves to prevent arc-suppression diodes from appearing in the Diode Report (see paragraph 3.6.2.3e). The intent of the Diode Report is to list blocking diodes only, as these control current flows through the network tree.

A.6 Impedance

Very little significance is attached to impedance values in the Automated Sneak Program at this time. Nominal values may be included in the BID for subsequent reference. The BID values are taken to be in thousands of ohms. Therefore, the specified impedance may range from 00.1 K Ω to 99.9 K Ω . It is common usage to specify 00.1 K Ω for unknown values suspected to be of low impedance and 99.9 K Ω for unknown high impedances. The coded value must always be numeric.

A.7 Remarks

The remarks field of the B2 input is used to provide abbreviated notes regarding the branch or tree for reference during subsequent utilization of the reports and analysis. Remarks should always be provided for switches, loads, diodes, relay coils, special nodes, power and ground points. The remark should indicate functions, source and type of power, type of ground, or other information pertinent to the subsequent network tree analysis. Remarks may even be used to explain special code techniques and to specify reference drawing zone locations. While remarks are important on appropriate branches, it should be kept in mind that only the Path Report will show remarks for intermediate segments in a tree, and this report is used for reference only. It is not normally used during construction or analysis of the tree. Therefore, remarks should generally be given on those segments which will appear in one of the derived reports: Terminal Branch Report, Switch Branch Report, Load Report, Diode Report, or Special Node Cross-Reference Report (see Paragraph 3.6.2.3b-f).

END